Thermal Enhancements for Separable Thermal Mechanical Interfaces

Matt Flannery[1], James Schmidt[2], and Jens Weyant[3]
Advanced Cooling Technologies, Inc., Lancaster, PA, 17601, USA

and

Kevin Thorson[4]
Lockheed Martin – Advanced Technology Laboratories, Eagan, Minnesota, 55121, USA

Aerospace and defense computing requirements are becoming more demanding as the focus on network-centric warfare, the use of graphics and digital signal processing, data acquisition, and other computer-intensive tasks increases. Future designers will be tasked with providing improved systems but will be restricted by the thermal resistance of current electronics enclosures. Therefore, enhancements in thermal management will be paramount for increasing computing capabilities. In the current state-of-the-art, slice-form electronics cards are fastened to chasses with embedded heat sinks by a separable thermal mechanical interface (STMI), also referred to as wedgelocks or card retainers. The STMI provides a mechanical connection that fixes the card in the chassis and provides a thermal path for heat rejection. However, the high thermal impedance STMI produces a thermal bottleneck to heat rejection from the electronics components and requires improvement to enable the increase in computing power requirements. Advanced Cooling Technologies, Inc., in collaboration with Lockheed Martin – Advanced Technology Laboratories, have developed a thermally enhanced STMI that produces a secondary heat rejection path with a 50% lower thermal resistance than current systems by maximizing the heat transfer surface area. Thus, this technology, in conjunction with high thermal conductivity electronics cards, can reduce the thermal bottlenecks that limit current heat rejection capacity, and subsequently power output, of electronics components in aerospace and defense computing systems.

Nomenclature

R	=	thermal resistance
T_i	=	temperature of the i^{th} component
$\dot{Q}_i$	=	thermal power
$\dot{m}$	=	mass flow rate
c_p	=	specific heat capacity
EB	=	energy balance
I	=	current
V	=	voltage
ΔT_i	=	temperature difference
ω_i	=	uncertainty in the i^{th} measurement
$MTTF$	=	mean time to failure
E_a	=	activation energy
k	=	Boltzman's constant

[1] Lead Engineer, Defense Aerospace Research and Development Group, 1046 New Holland Ave. Lancaster, PA 17601
[2] Research and Development Engineer, Defense Aerospace Research and Development Group, 1046 New Holland Ave. Lancaster, PA 17601
[3] Lead Engineer, Defense Aerospace Product Development Group, 1046 New Holland Ave. Lancaster, PA 17601
[4] Sr. Staff Research Engineer, Advanced Technology Laboratory, 1303 Corporate Center Drive, Eagan, MN 55121

I. Introduction

Aerospace and defense computing requirements are becoming more demanding with the focus on network-centric warfare, the increasing use of graphics and video, digital signal processing, sensor data processing, and generally more computer-intensive applications.[1] With the system architecture upgraded to increase the capacity and allow easy replacement, the issue of cooling becomes even more challenging given the increased power consumption. For example, the previous VMEbus slot was limited to a maximum of 90 W at 5 V, whereas the new VPX slot allows for up to 115 W at the same voltage, or up to 384 W at 12 V or 768 W at 48 V.[2]

To provide system flexibility and maintainability, electronics components are mounted to a thermally conductive card module. The card module is secured into a chassis by separable thermal mechanical interfaces (STMI), also referred to as a wedgelock, as shown in Figure 1. The waste heat generatred from the electronics components is conducted along the card module to the chassis wall where it is ultimately rejected.

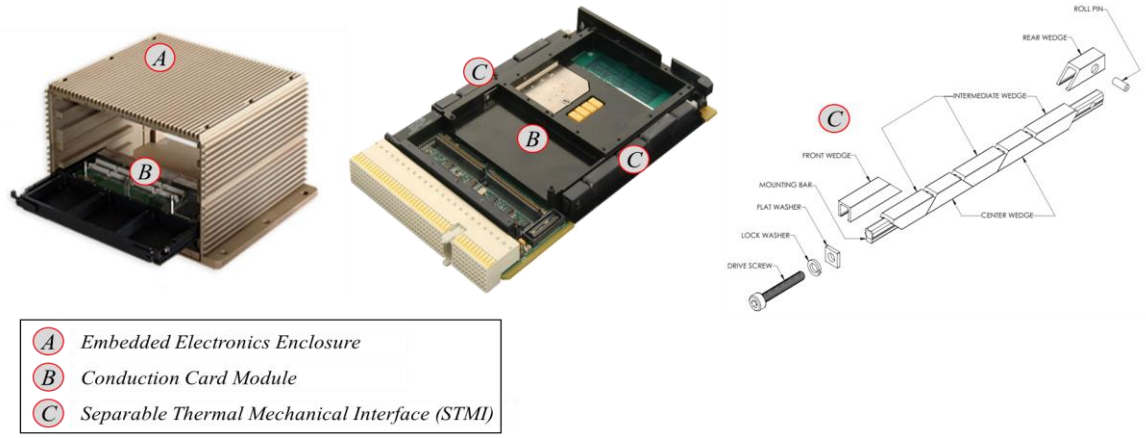

Figure 1. Embedded Electronics Assemblies used in Aerospace and Defense Applications. A Conduction Cooled Card *(B)* is Installed into an Enclosure *(A)* and Secured by STMIs *(C)*.

Current STMIs, as shown in Figure 1c, use a series of wedged interfaces that are mounted to a common rail. A screw engages with the rail and pushes a plate washer that advances the wedges. As the screw is tightened to a torque specification, the wedges expand perpendicularly from the common rail, and this expansion of the wedges applies pressure between the card module flange and chassis rail to mechanically lock the card into the chassis. While making the mechanical connection to lock the card in the chassis, the wedgelock creates thermal paths to reject heat from the conduction card module to the chassis, as shown in Figure 2.

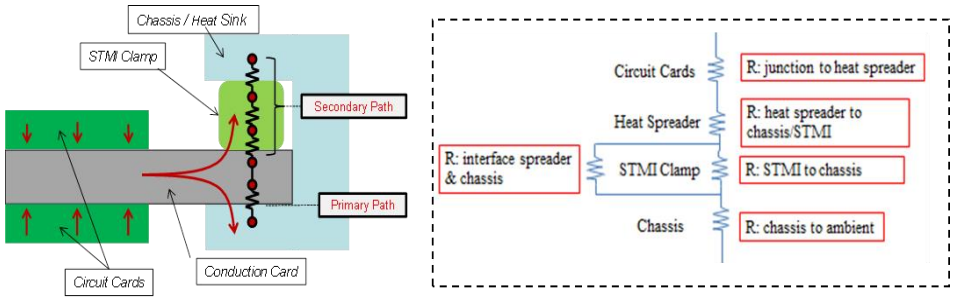

Figure 2. Cross-section inllustration of a typical conduction-cooled card and chassis assembly.

The conduction cooling capacity of the module is limited to the heat transferred from the card module to the chassis. This heat transfer occurs through a primary path formed between the card module flange and chassis rail interface, and through a secondary path created by the STMI, as shown in Figure 2. The heat transferred through the primary path is dependent on the thermal interface resistance between the card module flange and chassis rail which has a strong dependence on the applied pressure to the module flange by the STMI.[3] The heat transferred through the

secondary thermal path is dependent on the thermal design of the STMI. In current STMI designs, the heat transferred must pass through multiple wedge interfaces which gives rise to a large thermal impedance. At typical torque specifications, the ratio of heat transferred through the primary and secondary paths is approximately 70:30.[4] This produces a thermal bottleneck that requires improvement to reject heat from embedded electronics as total component power are projected to exceed 700 W.

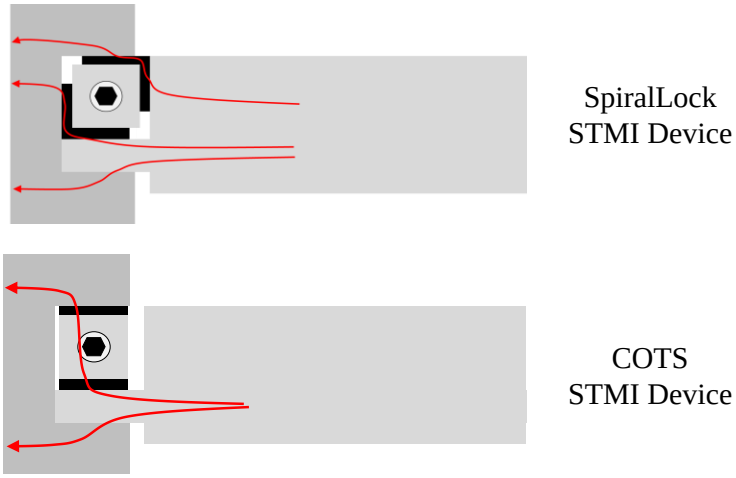

Figure 3. *(Top)* Illustration of the SpiralLock STMI Device exhibiting secondary thermal paths that bypass wedge interfaces. *(Bottom)* COTS STMI device exhibiting secondary thermal paths directly through the wedge interfaces.

The thermal performance of commercial off the shelf (COTS) STMIs is dependent on the applied pressure to the chassis rail and card module flange. However, with segmented wedge sections, the outward force is applied to discrete points along the length of the module flange, which produces a varying thermal interface resistance. Additionally, the wedge to wedge interfaces in the current STMI design produce high thermal impedance which limits conductive heat transfer through the device and along the secondary heat rejection path. Thus, to improve the thermal performance of the STMI, a uniform pressure must be applied to the entire length of the device to maximize surface area for heat transfer, a large outward force must be generated to minimize thermal interface resistances, and a favorable conduction path through the STMI must be established.

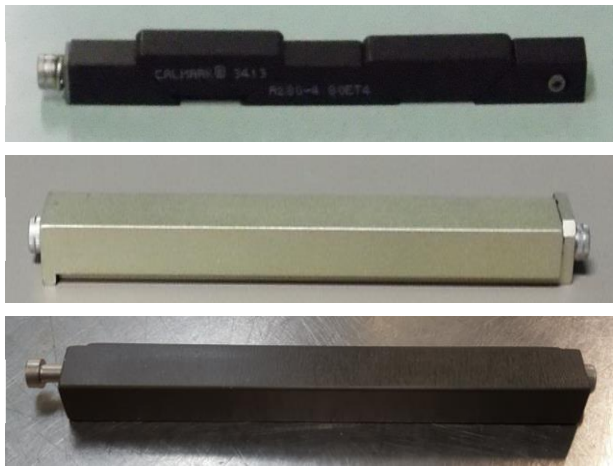

Figure 4. Comparison of COTS STMI, the Generation I SpiralLock, and Generation II SpiralLock STMI Designs.

To address these improvements, a novel STMI was designed based on the SpiralLock technology.[5] While current STMI's utilize a wedge angle on one plane, the SpiralLock design utilizes a wedge with a compound angle that causes expansion of the wedges on two axes to push L-brackets against the chassis wall and card module flange. This improvement not only increases the uniformity of the applied pressure to the chassis wall and card module flange, but provides a secondary thermal path that bypasses the wedge interfaces, as shown in Figure 3.

The first generation of the SpiralLock STMI was actuated from two bolts that were tightened from either side of the chassis, whereas the standard COTS STMIs are tightened from the front face of the chassis. While effective, the two sided bolting design was not compatible with current chassis designs. Thus, the second generation of the SpiralLock STMI, and the subject of the subsequent evaluations, was upgraded to enable single sided actuation that can be implemented into current systems that meet the ANSI/VITA 48.2 standards. Comparison of the COTS STMI, Generation I SpiralLock, and Generation II SpiralLock is presented in Figure 4. In this study, the applied pressure and thermal performance of the COTS STMI and SpiralLock STMI are evaluated and compared in simulated operating environments.

II. Experimental Test Apparatus Development

The thermal performance of the SpiralLock STMI is dependent on applying a uniform pressure along the length of the device and producing a low thermal impedance secondary heat transfer path from the card module to the chassis. Therefore, to evaluate performance improvement, the SpiralLock and COTS STMIs were tested for contact pressure uniformity and thermal resistance using custom test apparatus designed and fabricated as outlined below.

A. Contact Pressure Test Apparatus

The uniformity of the contact pressure across the key heat transfer interfaces in the SpiralLock and COTS STMI design, respectively, was evaluated by inserting pressure sensitive paper between the interfaces and tightening the STMI to a torque of 20 in-lbs. The pressure sensistive paper was then evaluated qualitatively for pressure uniformity and regions of isolated contact. For the SpiralLock STMI, the pressure sensitive paper was inserted between the top L-bracket and the top chassis rail, the top L-bracket and side of the conduction card, the bottom L-bracket and top of the conduction card module flange, the bottom L-bracket and the sidewall of the chassis, and the conduction card flange and bottom rail of the chassis. For the COTS STMI, the pressure sensitive paper was placed between the top rail of the chassis and the top of the STMI, the bottom of the STMI and the top of the conduction card module flange, and between the conduction card module flange and the bottom rail of the chassis. These key interfaces are outlined in Figure 5.

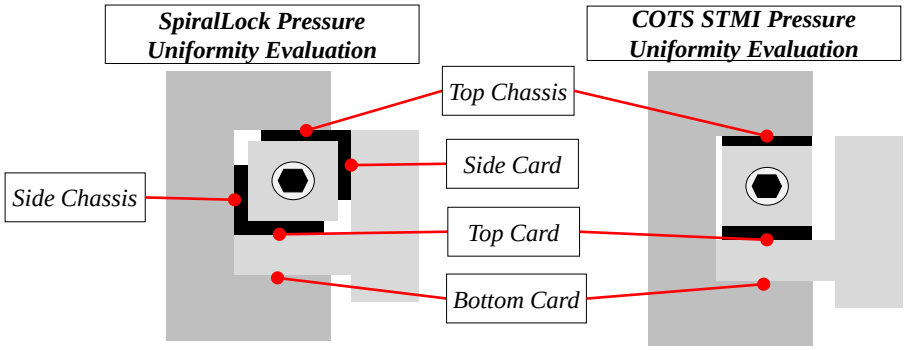

Figure 5. Locations of pressure sensitive paper for pressure uniformity evaluations.

B. Thermal Test Chassis

The thermal performance of the SpiralLock and COTS STMI was evaluated in a custom-built, liquid-cooled, three-card chassis, as shown in Figure 6. An aluminum conduction card was fabricated and a cartridge heater embedded heater block was attached to the middle of the card. The card was clamped into the middle rail of the chassis and coolant was pumped through the cold plates to ultimately reject the heat from the chassis. Coolant flow rate to each cold plate was monitored and recorded by flow meters and controlled by needle valves at the inlet to each cold plate. The inlet and outlet coolant temperatures were measured and recorded by platinum RTDs to provide calorimetry of the test apparatus and the coolant was returned to a thermal control unit where the inlet temperature of the coolant was maintained. A schematic of the thermal test chassis controls and instrumentation is presented in Figure 7 and operating conditions of the thermal test chassis are presented in Table 1. T-type thermocouples were placed throughout the conduction card and chassis

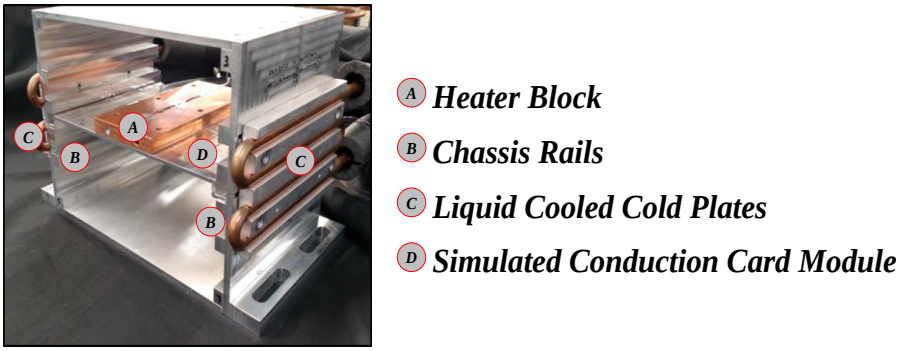

Figure 6. Thermal test chassis for evaluating the thermal performance of the SpiralLock and COTS STMI.

test apparatus, as shown in the thermocouple map in Figure 7 to monitor and record key temperatures for thermal evaluations.

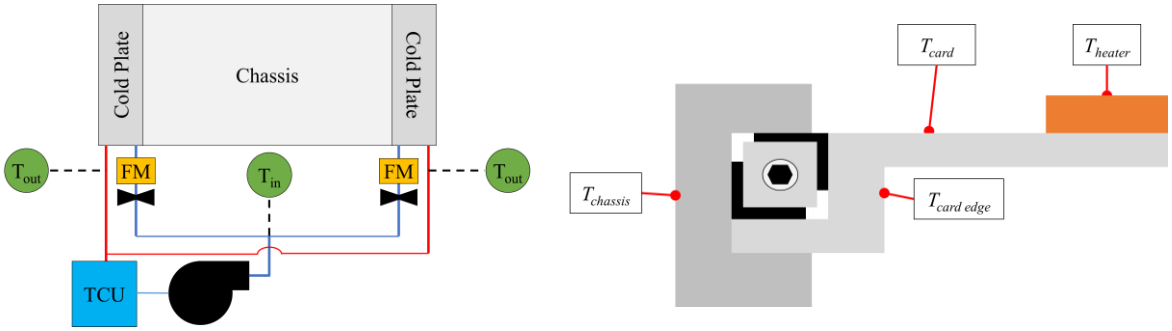

Figure 7. (*Left)* Schematic of the Thermal Test Chassis for Evaluating the Thermal Performance of the SpiralLock and COTS STMI. *(Right)* Thermocouple map for the thermal performance evaluation of the SpiralLock and COTS STMIs.

The thermal performance of each STMI was evaluated by attaching the device to the conduction card flange, tightening to the specified torque, and measureing the thermal resistance between the card and chassis at the designated heater power. The thermal resistance of the STMI interface was calculated by Eq. (1), where $T_{cardedge}$ and $T_{chassis}$ are the temperature of the card and chassis, respectively, and $\dot{Q}_{removed}$ is the thermal power removed through the STMI interface. The power removed through each wall of the chassis is calculated through calorimetry of the cold plate by Eq. (2), where $\dot{m}$ is the mass flow rate of coolant, C_p is the specific heat capacity of the coolant, and T_{outlet} and T_{inlet} are the coolant outlet and inlet temperatures of the cold plate, respectively.

Table 1. Thermal Test Chassis Operating Parameters

Operating Parameter	Value
Inlet Coolant Temperature	*25°C*
Coolant Flow Rate	*0.09 GPM*
Heater Power	*200 W*
Installation Bolt Torque	*5-15 in-lbs*

$$R = \frac{(T_{cardedge} - T_{chassis})}{\dot{Q}_{removed}} \quad (1)$$

$$\dot{Q}_{removed} = \dot{m} c_p (T_{outlet} - T_{inlet}) \quad (2)$$

$$EB\% = \frac{|\dot{Q}_{addition} - \dot{Q}_{removed}|}{\dot{Q}_{addition}} = \frac{|IV - \dot{m} c_p (T_{outlet} - T_{inlet})|}{IV} \quad (3)$$

To ensure accurate performance of the test apparatus and elimination of heat losses, the heat flow through the test chassis was evaluated and thermal test data was only collected when the energy balance agreed within 10%. The energy balance was calculated from Eq. (3), where $\dot{Q}_{addition}$ is the electrical power to the heater block on the card, and I and V are the electrical current and voltage to the heater block, respectively.

The uncertainty in the thermal resistance calculation due to the propogation of error in experimental measurements was calculated by Eq. (4), where ω_R is the uncertainty in the thermal resistance, ΔT_{STMI} is the temperature difference between the conduction card edge and chassis, $\dot{Q}_{removed}$ is the heat removed through the cold plates, $\omega\dot{Q}_{removed}$ is the uncertainty in the heat removed, and $\omega\Delta T_{STMI}$ is the uncertainty in the temperature difference across the STMI.[6] The uncertainty in the temperature difference across the STMI was calculated from Eq. (5) where $\omega T_{card\ edge}$ and $\omega T_{chassis}$ is the uncertainty in the card edge temperature and chassis temperature, respectively. The uncertainty in the heat removed was calculated from Eq. (6), where $\omega\Delta T_{coolant}$ is the uncertainty in the temperature rise of the coolant across the cold plate, and the $\omega\dot{m}$ is the uncertainty in the mass flow rate measurement. The uncertainty in the temperature rise of the coolant was calculated from Eq. (7), where ωT_{inlet} and ωT_{outlet} is the uncertainty in the inlet and outlet coolant temperatures, respectively.

$$\omega_R = \sqrt{\left(\frac{\Delta T_{STMI}}{\dot{Q}_{removed}^{\ 2}}\right)^2 \cdot \left(\omega \dot{Q}_{removed}\right)^2 + \left(\frac{1}{\dot{Q}_{removed}}\right)^2 \cdot (\omega \Delta T_{STMI})^2} \quad (4)$$

$$\omega_{\Delta T_{STMI}} = \sqrt{\left(\omega T_{card\ edge}\right)^2 + (\omega T_{chassis})^2} \quad (5)$$

$$\omega_{\dot{Q}_{removed}} = \sqrt{\left(\dot{m} c_p\right)^2 \cdot (\omega \Delta T_{coolant})^2 + \left(c_p \Delta T_{coolant}\right)^2 \cdot (\omega \dot{m})^2} \quad (6)$$

$$\omega_{\Delta T_{coolant}} = \sqrt{\omega T_{inlet}^2 + \omega T_{outlet}^2} \quad (7)$$

The unceratiny in the card and chassis temperature measurements, the coolant temperature measurements, and coolant flow rate was 0.5°C, 0.2°C, and 0.006 GPM, and the density and specific heat capacity of the coolant were considered to be certain at the operating temperatures of the test. Therefore, the thermal resistance of the STMI interface was able to be determined within an experimental uncertainty of 10%.

III. Data/Results

A. Contact Pressure Testing

The effectiveness of the thermal performance STMIs is dependent on the uniformity of the contact pressure across the device. Isolated points of pressure will impede heat flow by reducing contact area between the conduction card module and chassis rail. Thus, the uniformity of the contact pressure was evaluated by the pressure sensitive paper testing outlined above and results for the SpiralLock and COTS STMIs are presented in Figure 8.

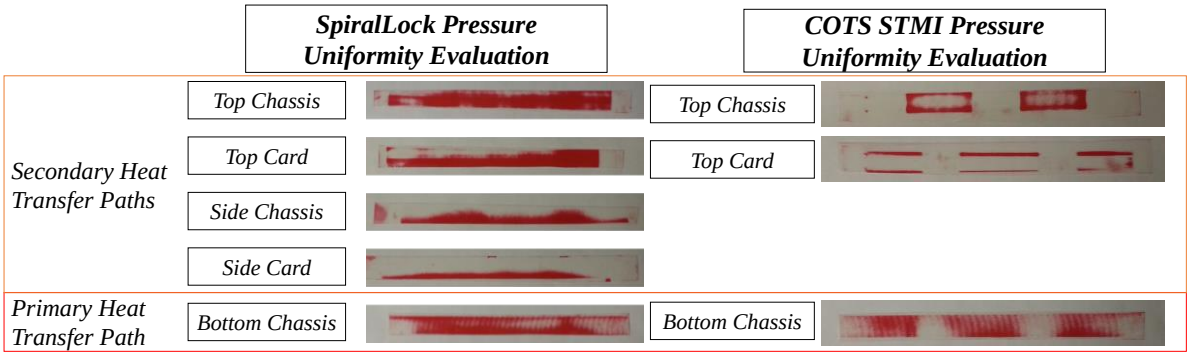

Figure 8. (*Left)* Pressure sensitive paper test results for the SpiralLock STMI. *(Right)* Pressure sensitive paper test results for the COTS STMI.

As shown in Figure 8, the primary heat transfer path formed by the COTS STMI (labeled *Bottom Chassis),* exhibits regions of isolated contact, whereas the SpiralLock STMI exhibits a more uniform pressure applied across the device. Additionally, the secondary heat transfer paths exhibit a greater total contact area for the SpiralLock than the COTS STMI and are attributed to the greater number of heat transfer contact surfaces and uniform application of pressure from the L-brackets. Thus, the more uniform pressure and greater total contact area of the SpiralLock design is expected to improve the thermal performance of both the primary and secondary heat transfer paths.

B. Thermal Performance Testing

STMIs are currently a thermal bottleneck in aerospace and defense computing applications. Thus, to enable increased power capabilities of electronics components, the thermal performance of STMIs requires improvement. To evaluate the ability of the SpiralLock to relieve this thermal bottleneck was evaluated in the thermal test chassis outlined above. The thermal resistance of the SprialLock and COTS STMIs was measured at increasing bolt torque from 5 to 15 in-lbs and results are presented in Figure 9.

As shown in Figure 9, the thermal resistance of the SpiralLock was approximately 50% less than the COTS STMI at all bolt torque conditions evaluated. This reduction in thermal resistance indicates that the secondary thermal path provided by the SpiralLock design is a lower thermal impedance path than the COTS STMI design, thereby improving heat rejection from the conduction card module. The improvement in thermal resistance is supported by the pressure uniformity data presented above wherein the secondary thermal path produces an increased surface area for heat rejection from the conduction card to the chassis. Thus, the SpiralLock STMI reduces the current thermal bottleneck in aerospace and defense computing applications and supports the advancement of computing power in these systems.

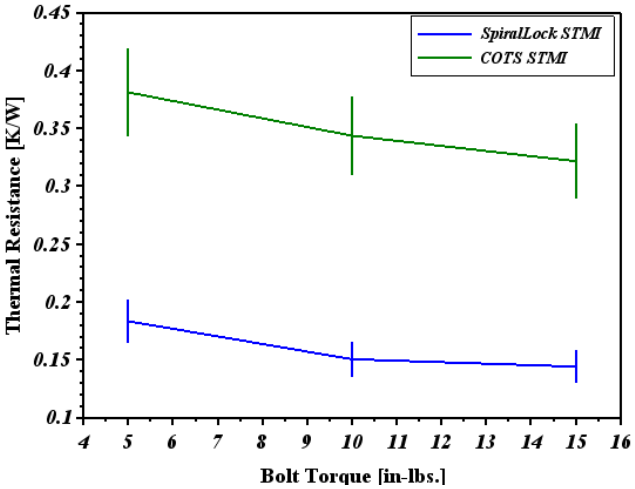

Figure 9. Thermal resistance of the the SpiralLock and COTS STMI at varying bolt torque.

IV. Discussion

The SpiralLock STMI demonstrated a reduction in thermal resistance from the conduction card module to the chassis by 50% when compared to COTS STMIs. This improvement alleviates a thermal bottleneck in aerospace and defense computing systems that are trending towards higher power. Utilizing this technology not only supports next generation, higher power systems, but also can be directly implemented into current systems to reduce component temperatures thereby extending lifetime and reliability. For example, a current conduction card module with a total heat rejection of 100 W assuming symmetric heat dissipation (*i.e.* 50 W transferred per interface), will reduce the operating temperature of the electronics components by 10°C when exchanging the COTS STMI for a SpiralLock.

$$LTI = \frac{MTTF_2}{MTTF_1} = e^{\left(\frac{E_a}{k}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right)} \qquad (8)$$

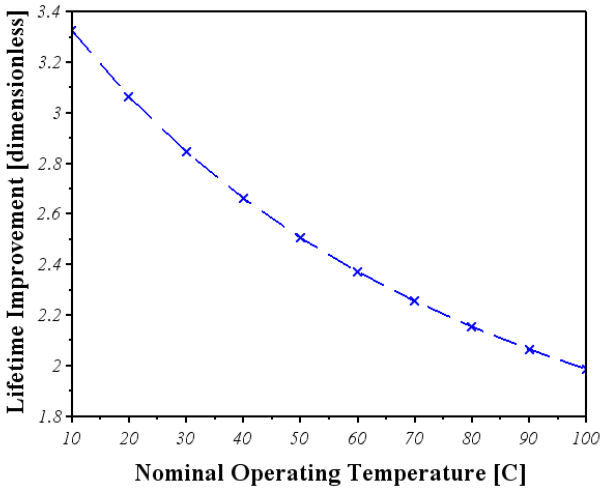

Figure 10. Lifetime improvement of 100 W electronics component when operating temperature is reduced by 10°C.

Thus, the improvement in the lifetime of the electronics components can be estimated by modification of Black's equations in Eq. (8), where *LTI* is the lifetime improvement, *MTTF* is the mean time to failure, E_a is the activation energy (0.8 eV), k is the Boltzmann's constant, and T_1 is the nominal operating temperature when using COTS STMIs and T_2 is the operating temperature when using a SpiralLock STMI (*i.e.* T_1-10°C). [7] The lifetime improvement for a 100 W component as outlined above, is presented as a function of nominal operating temperature in Figure 10. This analysis demonstrates that utilizing the SpiralLock STMI can decrease operating temperatures and increase the lifetime of electronics components that require 100 W of waste heat rejection by 2-3×. Thus, with the reduction in thermal resistance between the conduction card module and chassis interface, the SpiralLock STMI can support the increase in power of electronics components or be utilized to increase lifetime of reliability of current computing systems.

V. Conclusion

The increase in component power in aerospace and defense computing systems requires and increase in thermal performance of conduction cooled chassis. Currently, the separable thermal mechanical interface is a thermal bottleneck that impedes the efficient rejection of heat from electronics components. An STMI based on the SpiralLock design that maximizes surface area for heat rejection was developed to directly integrate with current ANSI/VITA 48.2 compliant systems and reduce the thermal impedance at this interface. Pressure uniformity evaluations demonstrated a significant increase in the total surface area for heat rejection compared to the COTS design, which resulted in a 50% reduction in the thermal resistance under simulated operating condition. This reduction in thermal resistance would produce a 10°C reduction in operating temperature of electronics components that require 100 W of heat dissipation. As a result, the lifetime of the electronics components can be increased by approximately 2-3× at current operating temperatures. Thus, utilization of the SpiralLock technology can not only support the increased power loads of next generation systems, but also improve the reliability of currently deployed systems.

Acknowledgments

The authors would like to acknowledge Dr. Brenton Taft for his support through these developments which were funded under United States Air Force Research Laboratory Space Vehicles Directorate Contract No. FA9453-15-C-0418.

References

[1] GE Fanuc Embedded Systems, "VPX: VMEbus for the 21st Century", 2007.

[2] Allen, Roger. "All Aboard!" Electronic Design 26 June 2008: 28-35.

[3] M.M. Yovanovich and V.W. Antonetti, *Application of Thermal Contact Resistance Theory to Electronic Packages*, Advances in Thermal Modeling of Electronic Components and Systems, Vol. 1, Editors A. Bar-Cohen and A.D. Kraus, Hemisphere Publishing Corporation, 1988, pp. 79-128.

[4] Campo, Darren, Jens Weyant, and Bryan Muzyka. "Enhancing Thermal Performance in Embedded Computing for Ruggedized Military and Avionics Applications." Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm) (2014)

[5] Monson, Robert J., Kevin J. Thorson, Melissa A. Grette-Compton, and Kent D. Katterheinrich. Cardlock Clamp. Lockheed Martin Corporation, assignee. Patent US8559178B2. 15 Oct. 2013.

[6] Holman, J. P., and Walter J. Gajda. *Experimental Methods for Engineers*. New York: McGraw-Hill, 1978.

[7] W.J. Choi, et al. Mean-time to failure of flip chip solder joints on Cu/Ni(V)/Al thin-film under-bump-metalization. Journal of Applied Physics. Volume 94, Number 9. November 1st, 2003.